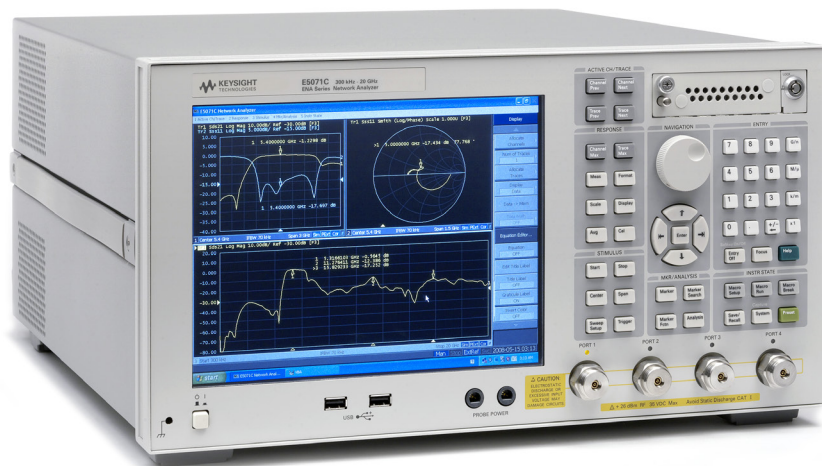


Keysight Technologies

E5071C ENA Option TDR

Enhanced Time Domain Analysis

Technical Overview



Introduction

One box solution for high speed serial interconnect analysis

- Simple and Intuitive Operation
- Fast and Accurate Measurements
- ESD Robustness

Why choose ENA Option TDR for your toughest high speed serial interconnect measurement challenges?

As an engineer you're no stranger to tough challenges that help you to deliver high standards and meet your customer's needs better than anyone else can. But deploying your next design successfully is even more difficult when you're incorporating today's high speed serial technologies. Signal eyes become smaller and measurement error from your instrument becomes less tolerable. Keysight Technologies, Inc. is committed to providing the best measurement solutions for those tough measurement challenges.

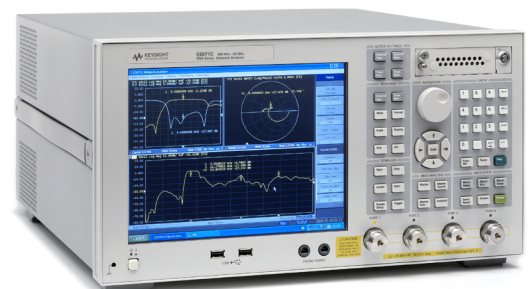
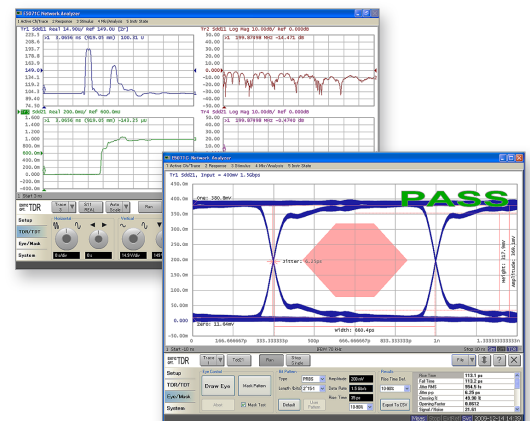
The Keysight ENA Option TDR provides the following three breakthroughs for signal integrity design and verification:

- Simple and Intuitive Operation
- Fast and Accurate Measurements
- ESD Robustness

Key features

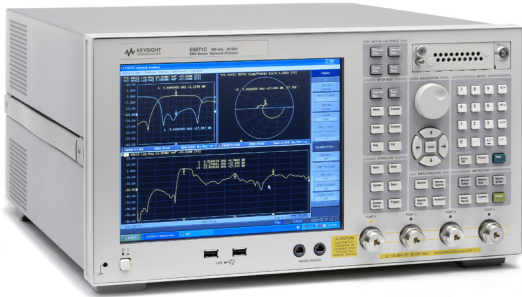
- Up to 20 GHz of bandwidth with 22.3 ps rise time enables measurement on the latest high speed serial standards
- Unmatched performance
 - Wide dynamic range to observe the true performance of your DUT: > 100 dB
 - Low noise floor for accurate and repeatable measurements: 20 uV rms
 - Fast measurement speed for real-time analysis: 41 msec at 1601 points with full 2-port calibration performed
- State-of-the art calibration techniques reduce measurement errors
 - Automatic deskew ensures easy removal of fixture and probe effects
 - Full calibration available for the utmost in measurement accuracy
- Upgrade all available ENA hardware and software options (bandwidth, number of ports, etc.) at any time

Inheriting the excellent accuracy from Keysight's E5071C ENA Vector Network Analyzer and adding the versatility of TDR oscilloscopes, the ENA Option TDR changes the world of TDR measurements.



Keysight E5071C ENA Option TDR

One-box solution for high speed serial interconnect analysis



As bit rates of digital systems increase, signal integrity of interconnects drastically affects system performance. Fast and accurate analysis of interconnect performance in both time and frequency domains become critical to ensure reliable system performance.

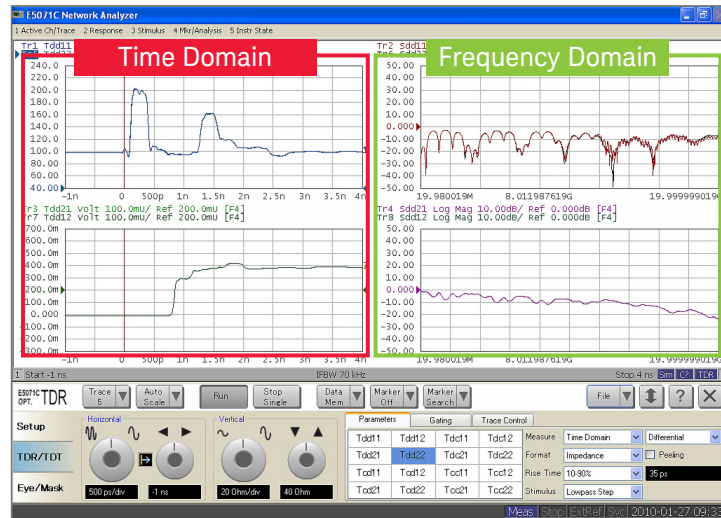
Because managing multiple test systems becomes difficult, a single test system that can fully characterize differential high speed digital devices is a very powerful tool

The ENA Option TDR provides an one box solution for high speed interconnect analysis, including impedance, S-parameters, and eye diagrams.

TDR/TDT Mode

TDR oscilloscope look-and-feel

The graphical user interface is design to provide a similar look-and-feel to traditional TDR oscilloscopes. You can easily set up complex measurements and quickly retrieve measurement data.



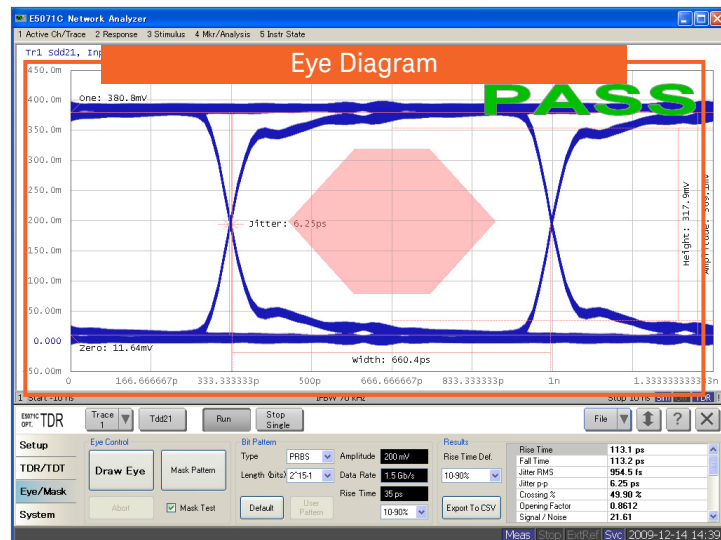
TDR/TDT and Eye/Mask Modes

Quickly change between observing the eye to making fast and accurate TDR/TDT and S-parameter measurements with a single mouse click.

Eye/Mask Mode

Dedicated controls for common adjustments

Software knobs provides simple controls for commonly used functions.



Keysight E5071C ENA Option TDR

One-box solution for high speed serial interconnect analysis

TDR/TDT Mode

Up to 9 markers

Zooming

Rise time

Dedicated controls for common adjustments

Automatic display allocation for most common measurement parameters depending on selected device topology

Flexibility to set measurement parameter for each individual trace

Set rise time to characterize expected performance at slower edge speeds

Δ Time (skew) measurements

Features

- Quickly obtain accurate TDR/TDT and S-parameter measurements
- Easily locate source of loss, reflections and crosstalk by simultaneous analysis of both time and frequency domains
- Single connection forward and reverse transmission and reflection measurements
- All possible modes of operation (single-ended, differential, and mode conversion)
- Measure just your device by utilizing advanced calibration techniques to remove cable, fixture, and probe effects

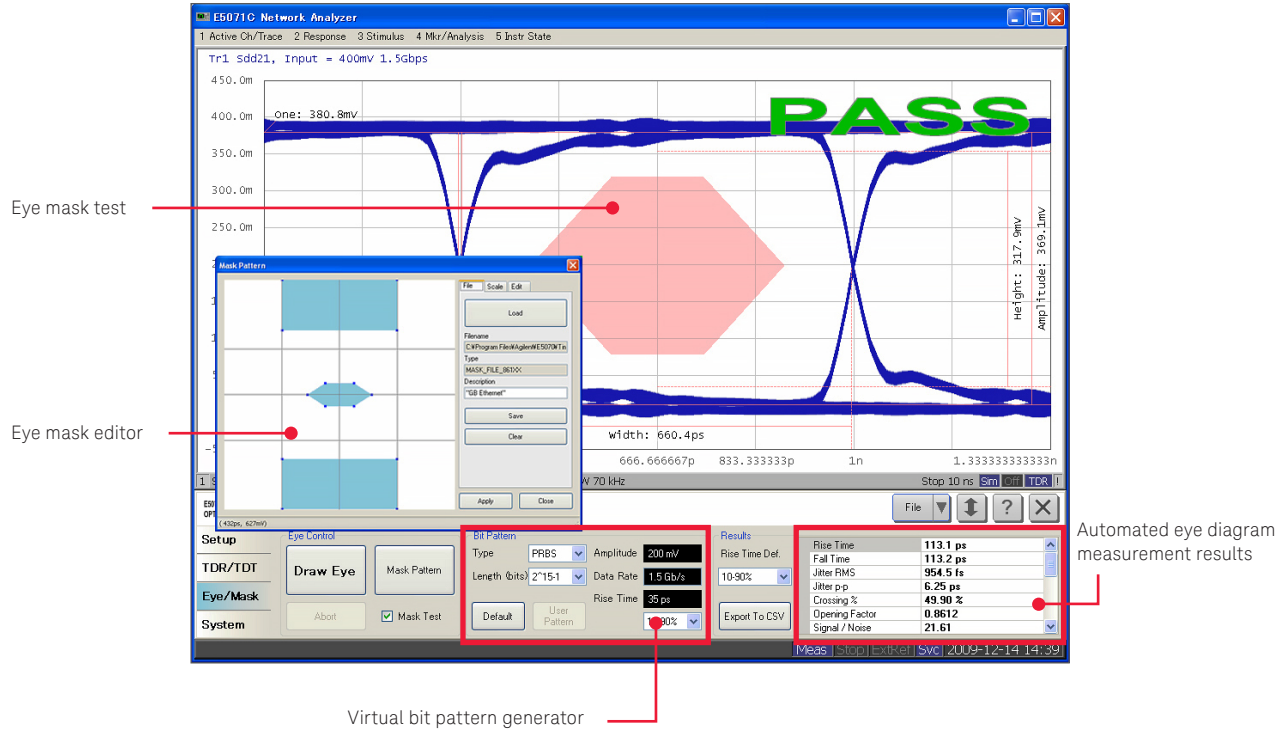
As bit rates of digital systems increase, the combination of both time domain and frequency domain analysis becomes important to ensure reliable system performance.

The ENA Option TDR provides simultaneous analysis of both time and frequency domains. The ENA Option TDR measures the characteristics of a test device as a function of frequency. The frequency domain information is used to calculate the inverse Fourier transform for time domain results.

Keysight E5071C ENA Option TDR

One-box solution for high speed serial interconnect analysis

Eye/Mask Mode



Features

- Gain insight into high speed interconnect performance through simulated eye diagram analysis
- Apply industry standard (PRBS, K28.5), or user specified patterns using the virtual bit pattern generator
- Predefined masks for many high speed serial standards
- No need for pulse generators as the eye diagram is synthesized from measurement results
- Determine optimal emphasis and equalization settings for your link
- Simulate real-world signals through jitter insertion

The ENA Option TDR provides simulated eye diagram analysis capability, eliminating the need for a hardware pulse pattern generator. The virtual bit pattern generator is used to define a virtual bit pattern. The defined bit pattern is then convolved with the device impulse response to create an extremely accurate measurement based eye diagram.

Efficient, high-throughput waveform compliance testing with a suite of predefined standards based eye diagram masks is possible with ENA Option TDR. Other eye diagram masks are easily created through scaling the predefined masks, editing existing masks, or creating new masks from scratch.

Keysight E5071C ENA Option TDR

Comprehensive signal integrity measurement solution for next generation high speed digital standards

With the increase in bit rates, standards continue to evolve and new measurements are often the result. There is a growing need in the industry for more thorough evaluation of components, as well as evaluation under actual operating conditions.

The ENA Option TDR offers a variety of measurement capabilities, providing you tools to characterize high speed digital designs more thoroughly.

- Determine optimal emphasis and equalization settings for your link
- Simulate real-world signals through jitter insertion
- Impedance analysis of active devices under actual operating conditions with Hot TDR measurements

Advanced waveform analysis features

Determine optimal emphasis and equalization settings for your link

A transmitter sends a serial signal over a transmission channel, such as backplanes and cables, to a receiver. As the signal data rate increases, the channel distorts the signal at the receiver. This distortion can cause a partially or completely closed eye diagram that makes it impossible for the receiver to extract the data. To recover the data from the eye diagram, it must be re-opened. This is where emphasis and equalization can help.

Emphasis and equalization are commonly used signal conditioning techniques when transmitting signals at gigabit data rates. The term emphasis is used to describe signal conditioning on the transmitter, while the term equalization is used on the receiver side.

Open up closed eyes by simulating emphasis and equalization via a simple GUI.

The image displays two screenshots of the 'Advanced Waveform' software interface, showing the configuration of signal conditioning blocks in a transmission channel model.

Top Screenshot: Emphasis Configuration

- Block Diagram:** Tx → Jitter → Emphasis → Differential DUT → Equalization → Rx. A 'De-embedding' block is also present between the DUT and Equalization.
- Emphasis Settings:**
 - Enable:
 - Cursor Level:
 - Pre Cursor: 0 dB
 - Post 1 Cursor: -3.5 dB
 - Post 2 Cursor: 0 dB
- Equation (CTLE):**

$$H(s) = \frac{K(s + \omega_z)}{(s + \omega_{p1})(s + \omega_{p2})}$$

$$K = A_{dc} \frac{\omega_{p1} \omega_{p2}}{\omega_z}$$

A_{dc} : DC Gain
- Waveform:** A differential eye diagram is shown with cursors indicating signal levels.

Bottom Screenshot: Equalization Configuration

- Block Diagram:** Same as the top screenshot.
- Equalization Settings:**
 - Enable:
 - Type: Equation File
 - Equation (CTLE):
 - DC Gain: 667 m
 - Zero Freq: 650 MHz
 - Pole1 Freq: 1.95 GHz
 - Pole2 Freq: 5 GHz
- Equation (CTLE):**

$$H(s) = \frac{K(s + \omega_z)}{(s + \omega_{p1})(s + \omega_{p2})}$$

$$K = A_{dc} \frac{\omega_{p1} \omega_{p2}}{\omega_z}$$

A_{dc} : DC Gain
- Waveform:** A differential eye diagram is shown, which appears more open than in the top screenshot.

Keysight E5071C ENA Option TDR

Comprehensive signal integrity measurement solution for next generation high speed digital standards

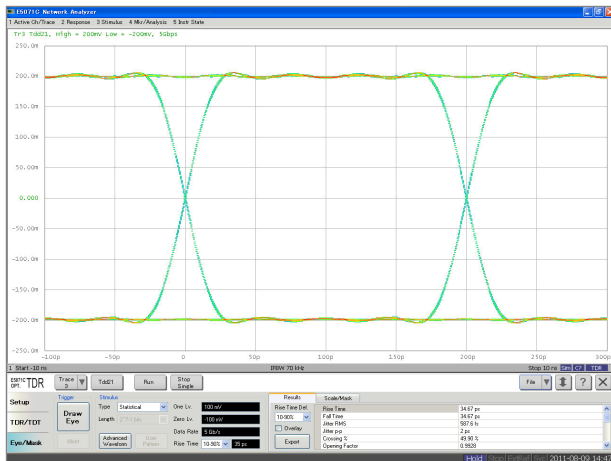
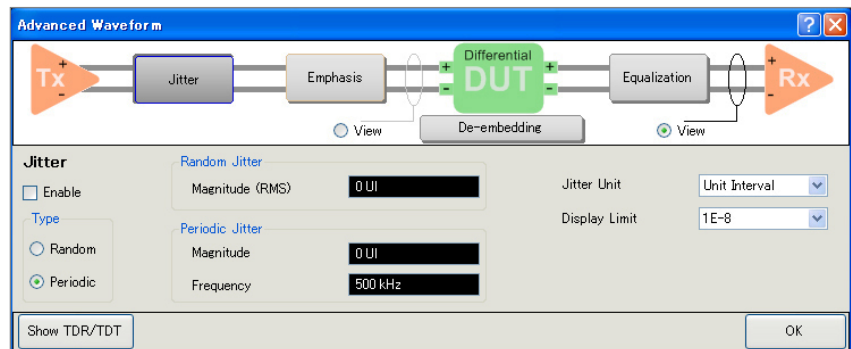
Advanced waveform analysis features

Simulate real-world signals through jitter insertion

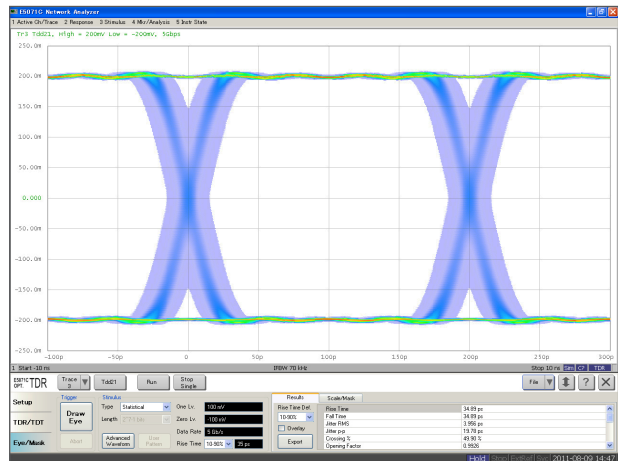
Interconnects can be characterized by measuring parametric characteristics such as loss and reflection. One challenge with such characterization is how to translate the measurements into what the eye diagram will look like at the end of a link. Another approach is to measure the interconnect driven by the expected worst case performance of the transmitter. This has the advantage of allowing direct measurement of eye characteristics at the end of the link. This process is called stressed eye testing.

If the interconnect can correctly transmit a stressed signal with eye characteristics equal to or better than what is specified at the receiver, then it should operate with the signal of any compliant transmitter. To this end, the stressed signal is composed of the worst-case compliant signal generated by the transmitter.

This precision stressed signal required to verify interconnect robustness can be realized with the jitter insertion feature of ENA Option TDR. Impairments such as random and periodic (sinusoidal) jitter can be configured.



Jitter OFF



Jitter ON (Random Jitter = 20 mUI)

Keysight E5071C ENA Option TDR

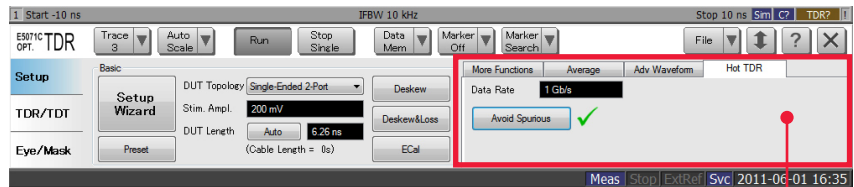
Comprehensive signal integrity measurement solution for next generation high speed digital standards

Hot TDR measurements

Impedance analysis of active devices under actual operating conditions

As bit rates of digital systems increase, impedance mismatch between components become a significant factor in system performance. A typical high speed digital system consists of a transmitter, interconnect, and receiver. As the transmitter signal reaches the receiver, any impedance mismatch at the receiver will cause some of the signal to be reflected back to the transmitter. Once the reflected signal reaches the transmitter, any impedance mismatch at the transmitter will cause re-reflections. Once this re-reflected signal reaches the receiver, it will cause eye closure.

Hot TDR is the TDR and return loss measurement of active devices in the power-on state.

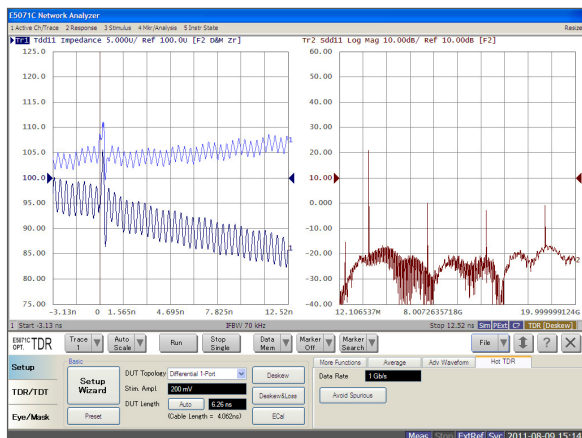


Hot TDR mode

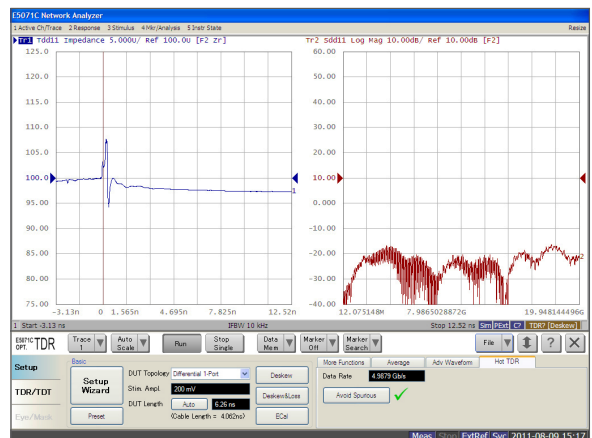
For Hot TDR measurements of transmitters (Tx), the Tx is powered on and outputting a data signal. The data signal from the Tx cause measurement error.

The ENA Option TDR implements a narrowband receiver architecture, which minimizes the effect from the Tx signal. But as the ENA Option TDR sweeps across the desired frequency range, there still may be frequencies where the spurious response from the Tx data signal overlaps the measurement frequency, causing measurement error.

The Avoid Spurious feature determines the spurious frequencies from the data rate (user input) and sets the optimum frequency sweep to minimize measurement error.



With the default setup, the data signal from the Tx causes fluctuations on the time domain response and spikes in the frequency domain response.



After Avoid Spurious operation, measurement errors due to the Tx data signal are minimized.

Keysight E5071C ENA Option TDR

Wide Range of Certified Compliance Test Solutions

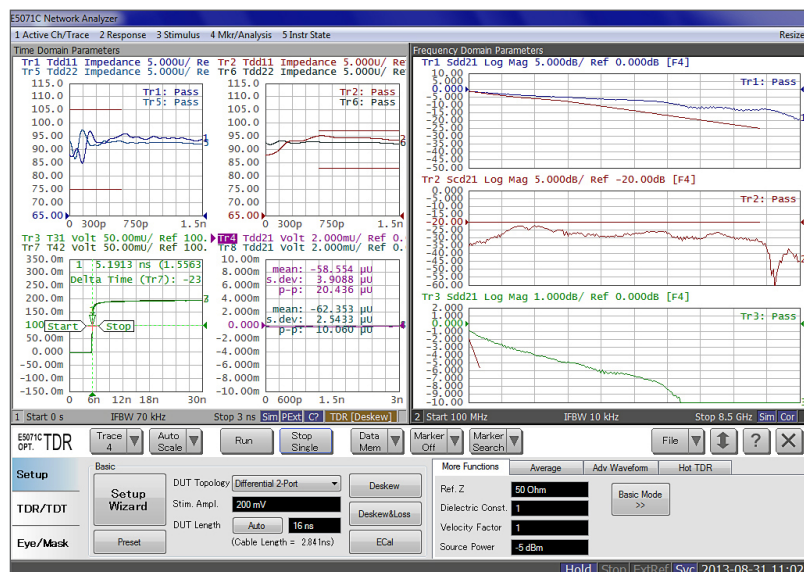
Today's demanding environment means you have much less time to understand the intricacies of the technologies you are testing. You also have less time to learn how to setup and operate test equipment. The ENA Option TDR compliance test solutions save you time and money with test solution overview presentations, standard specific setup files, and method of implementation (MOI) documents. The MOI is a step-by-step measurement procedure guide to support compliance testing for each standard and is provided to give you confidence you're running the right tests. Using the setup files and MOI documents, you can perform compliance tests efficiently with the ENA Option TDR. No longer do valuable resources need to be exclusively tied to learning and implementing the next standard – instead they can be deployed to designing the next big project.

The ENA Option TDR offers over 20 compliance test solutions and the list continues to grow.

Standards	MOIs & State Files		Test Solution Overview
	Cable-Connector Assembly	Tx/Rx Impedance	
USB	Available	–	Available
HDMI	Available	Available	Available
SATA	Available	Available	Available
DisplayPort	Available	–	Available
MIPI™	D-PHY	–	Available
	M-PHY	–	Available
Ethernet	10GBASE-TX	Available	–
	10GBASE-T	Available	–
	10GBASE-KR4/40GBASE-KR4	Available	Available
MHL	Available	–	Available
PCIe®	Available	–	Available
Thunderbolt	–	Available	Available
BroadR-Reach	Available	–	Available
SD Card	–	Available	–
Cfast	–	Available	–

Compliance test solutions that run on ENA Option TDR are certified to test to the exact specifications of each technology standard. If a test passes on the ENA Option TDR in your lab, you can be assured that it will pass in test labs and at plug fests worldwide. Keysight experts on technology boards and industry standards committees help define compliance requirements. As a result, you can be sure that the ENA Option TDR tools deliver to critical specifications.

For more information:
www.keysight.com/find/ena-tdr_compliance

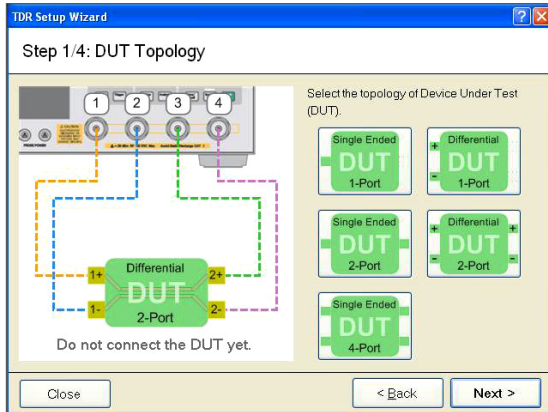


Three Breakthroughs for Signal Integrity Design and Verification

Simple and intuitive operation

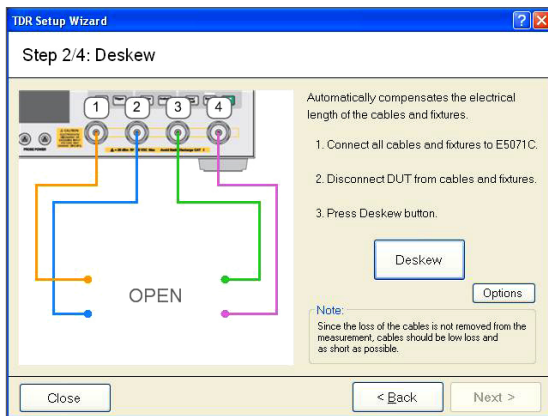
Complete device characterization with ENA Option TDR is straightforward. The graphical user interface has been designed provide a similar look-and-feel to traditional TDR oscilloscopes, providing intuitive operation even for users unfamiliar to vector network analyzers and S-parameter measurements.

A Setup Wizard guides the user through all of the required steps, making setup, error correction, and measurement intuitive and error-free.



Select DUT topology

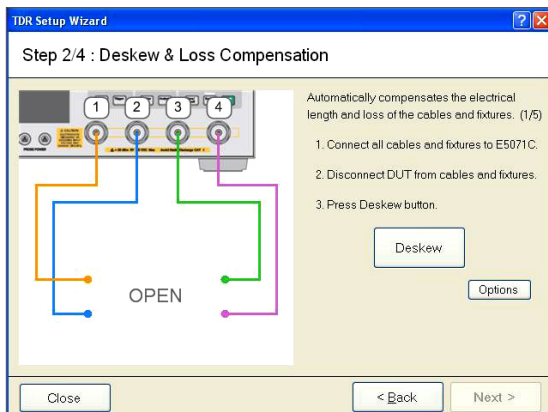
Select the topology of the device under test (DUT) . Single-ended 1-port, 2-port, 4-port and differential 1-port, 2-port topologies are supported.



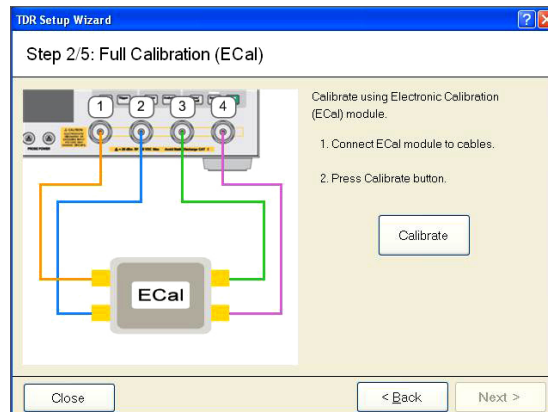
Perform error correction

Perform error correction by following the prompts. The prompts will differ depending on the error correction method selected.

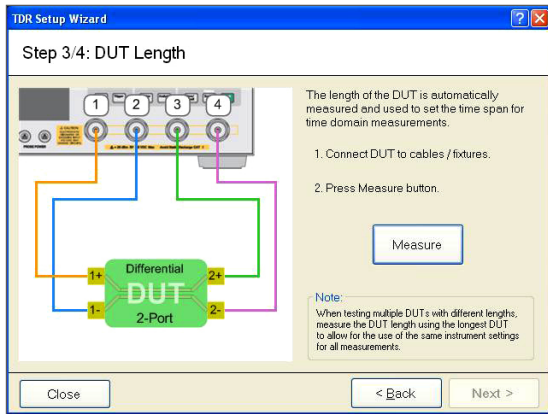
Deskew



Deskew and Loss Compensation



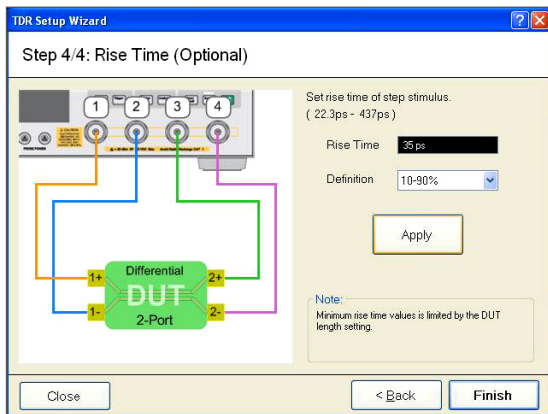
Full Calibration (Ecal)



Measure DUT length

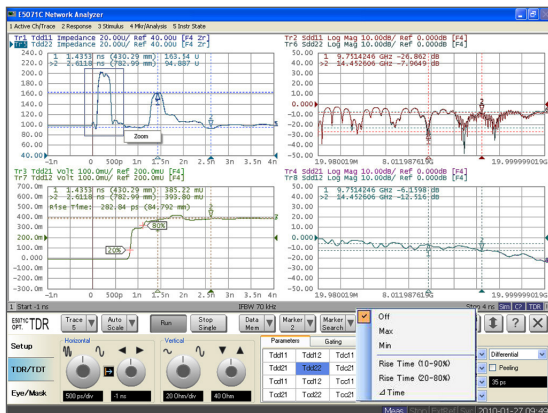
The length of the DUT is automatically measured and used to set the time base.

Tip: When testing multiple DUTs with different lengths, measure the DUT length using the longest DUT to allow for the use of the same instrument settings for all measurements.



Set Rise Time (optional)

Set rise time to characterize expected performance at slower edge speeds



Device measurement

The system is now ready to make all of the measurements required for complete device characterization.

ECal is an ideal solution for calibrating ENA Option TDR

Performing a full 4-port ECal takes far less than half the time and number of connections compared to using a mechanical cal kit. Furthermore, the accuracy of the calibration is comparable between electronic and mechanical methods. Traditional mechanical calibrations require intensive operator interaction which is prone to errors. With ECal, the operator simply connects the ECal module to the ENA Option TDR and the software controls the

Three Breakthroughs for Signal Integrity Design and Verification

Fast and accurate measurements

Error correction

Choose your level of accuracy – tradeoff between complexity and accuracy

Over the years, many different approaches have been developed for removing the effects of the test fixture and cables from the measurement. The level of difficulty for each error correction technique is related to the accuracy of each method. It is important to have a test system that will allow flexibility of choosing the method of error correction desired for each application.

Deskew (also known as Port Extension) mathematically extends the calibration reference plane to the DUT, effectively removing the delay from the test setup. This technique is easy to use, but assumes the cable and fixture – the unwanted structure – looks like a perfect transmission line: a flat magnitude response, a linear phase response, and constant impedance. If the cable and fixture are very well designed, this technique can provide good results.

Time domain gating is similar to port extension, in that it is also very easy and fast. The user simply defines two points in time or distance, and the software mathematically replaces the actual measured data in that section with data representing an “ideal” transmission line. The return loss is then recalculated to show the effects of the change in the frequency domain.

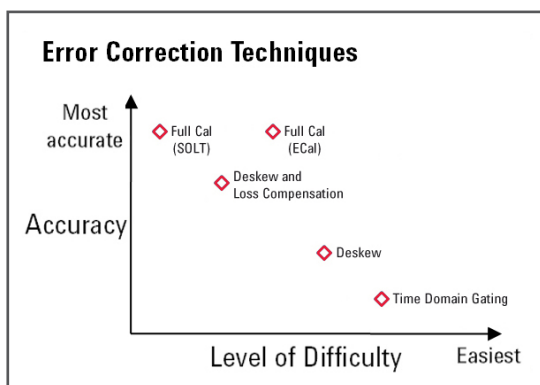
Deskew and loss compensation Mathematically extends the calibration reference plane to the DUT, effectively removing the delay and loss from the test setup. This technique is a good compromise between level of difficulty and accuracy.

Full calibration

Full calibration (Short/Open/Load/Thru (SOLT) calibration) type is one of the most comprehensive calibrations. This calibration effectively removes delay, loss, and mismatch from the test setup, making it possible to perform measurements with the highest possible accuracy.

Electronic calibration (Ecal)

ECal is a complete solid-state calibration solution. It makes calibration fast and easy.



Three Breakthroughs for Signal Integrity Design and Verification

ESD robustness

In applications such as electrical TDR circuit board testing and cable testing, large static charges can be stored in the DUT.

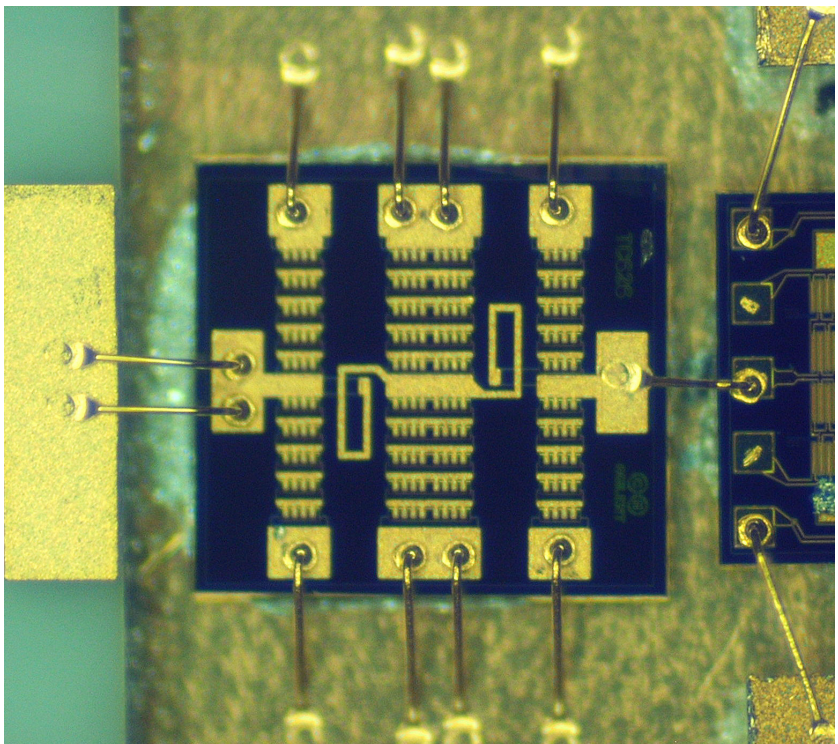
Special care is required when using traditional instruments in such situations, to make sure that the instrument is not damaged by electrostatic discharge (ESD). Vulnerability to ESD can lead to increased maintenance fees and long repair times.

The ENA Option TDR is designed for high robustness against ESD by implementing protection circuits inside the instrument.

Leveraging the company's expertise in RF design, Keysight has invested in key technology blocks like our proprietary ESD protection chip to significantly increase ESD robustness, while at the same time maintaining excellent RF performance.

To ensure high robustness against ESD, ENA Option TDR is tested for ESD survival according to IEC801-2 Human Body Model.

ESD Survival	IEC 801-2 Human Body Model. (150 pF, 330 Ω) RF Output Center pins tested to 3 kV, 10 cycles
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Interfaces and Accessories

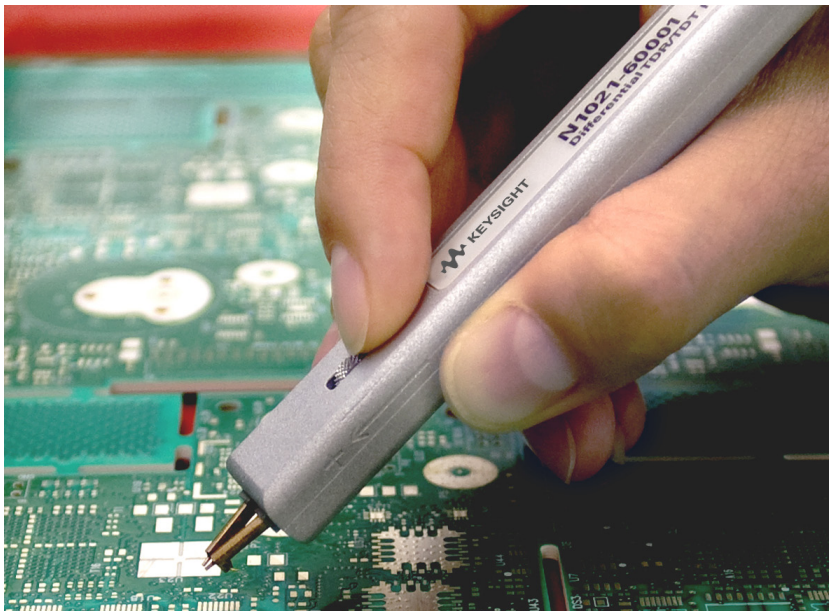
N1021B TDR/TDT Probe Kit

literature number 5990-4013EN

The Keysight N1021B Probe Kit includes an 18 GHz, 100 Ω differential input impedance, variable pitch, differential passive probe.

This ergonomically designed handheld probe interfaces the ENA Option TDR to printed circuit boards (PCBs) and components that lack common coaxial high frequency connectors.

The built-in wheel adjusts the pitch between the differential tips to make good contact to pads or access points spaced from closed to typical IC pins (2.54 mm).



Other Probes (3rd Party)

Keysight recommends using quality high performance probes with ENA Option TDR in order to minimize measurement degradation and variations.

Contact the following companies for alternative solutions:

- Cascade Microtech www.cmicro.com
- Inter-continental Microwave www.icmicrowave.com

Key Specifications

(Refer to E5071C ENA vector network analyzer data sheet for additional specifications.)

Test set Option	Category ¹	Option	Option	Option	Option	Option	Option	Option	Option	Option	Option
		2K5/4K5	2D5/4D5	280/480	285/485	260/460	265/465	240/440	245/445	230/430	235/435
Bandwidth	spec.	20 GHz	14 GHz	8.5 GHz		6.5 GHz		4.5 GHz		3 GHz	
Input Connector	char.	3.5 mm (male)		Type-N (female)							
Input Impedance	char.	50 Ω nominal									
Maximum Non-Destruct Voltage	typ.	\pm 35 VDC									
Maximum Test Port Input Voltage (Hot TDR Mode)	spec.	1.5 Vpp									
TDR Stimulus ²	char.	Step, Impulse									
TDR Step Amplitude ³	char.	1 mV to 5 V									
TDR Step Rise time (min) ⁴ (10% to 90%)	spec.	22.3 ps	31.9 ps	52.5 ps		68.6 ps		99.1 ps		149 ps	
TDR Step Response Resolution in free space ($\epsilon_r = 1$) (min) ⁵	char.	6.7 mm	9.6 mm	15.8 mm		20.6 mm		29.7 mm		44.7 mm	
TDR Impulse width (min) ⁴	spec.	30.2 ps	43.1 ps	71.0 ps		92.9 ps		135 ps		202 ps	
TDR Deskew Range (max) ⁶ (Test Cable Length)	spec.	50 ns									
DUT length (max) ⁷	spec.	416 ns		13.8 us	1.25 us	13.8 us	1.25 us	13.8 us	1.25 us	13.8 us	1.25 us
TDR Stimulus Repetition Rate (max)	spec.	20 MHz	14 MHz	8.5 MHz		6.5 MHz		4.5 MHz		3 MHz	
RMS Noise Level ⁸	SPD	20 μ Vrms									
Eye Diagram Data Rate (max) ⁹	spec.	16.0 Gb/s	11.2 Gb/s	6.8 Gb/s		5.2 Gb/s		3.6 Gb/s		2.4 Gb/s	

1. Specification (spec.): Warranted performance. All specifications apply at 23 °C (\pm 5 °C), unless otherwise stated, and 90 minutes after the instrument has been turned on. Specifications include guard bands to account for the expected statistical performance distribution, measurement uncertainties, and changes in performance due to environmental conditions. Typical (typ.): Describes performance that will be met by a minimum of 80% of all products. It is not guaranteed by the product warranty. General characteristics (char.): A general, descriptive term that does not imply a level of performance. Supplemental performance data (SPD): Supplemental performance data represents the value of a parameter that is most likely to occur; the expected mean or average. It is not guaranteed by the product warranty.
2. The time domain function of the ENA Option TDR is similar to the time domain reflectometry (TDR) measurement on a TDR oscilloscope in that it displays the response in the time domain. In the TDR oscilloscope measurement, a pulse or step stimulus is input to the DUT and the change of the reflected wave over time is measured. In the ENA Option TDR measurement, a sine wave stimulus is input to the DUT and the change of the reflected wave over frequency is measured. Then, the frequency domain response is transformed to the time domain using the inverse Fourier transform.
3. The TDR step amplitude setting does not vary the actual stimulus level input to the device, but is used when calculating the inverse Fourier transform.
4. Minimum values may be limited by the DUT length setting.
5. To convert from rise time to response resolution, multiply the rise time by c , the speed of light in free space. To calculate the actual physical length, multiply this value in free space by v_f , the relative velocity of propagation in the transmission medium. (Most cables have a relative velocity of 0.66 for a polyethylene dielectric or 0.7 for a PTFE dielectric.)
6. Using high quality cables to connect the DUT is recommended in order to minimize measurement degradation. The cables should have low loss, low reflections, and minimum performance variation when flexed.
7. Maximum DUT length is the sum of the DUT and test cable lengths. To convert from DUT length in seconds to distance in free space, multiply the value in time by c , the speed of light in free space. To calculate the actual physical length, multiply this value in free space by v_f , the relative velocity of propagation in the transmission medium. (Most cables have a relative velocity of 0.66 for a polyethylene dielectric or 0.7 for a PTFE dielectric.)
8. RMS noise level with 50 Ω DUT and default setup.
9. Maximum values may be limited by the DUT length setting.

Corrected System Performance

The specifications in this section apply to measurements made with the Keysight E5071C ENA vector network analyzer under the following conditions:

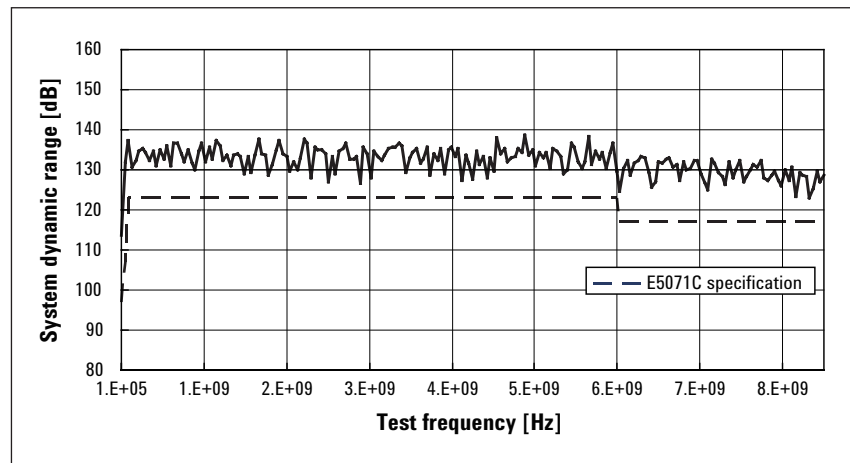
- No averaging applied to data
- Environmental temperature of 23 °C (± 5 °C) with less than 1 °C deviation from the calibration temperature
- Response and isolation calibration performed

System Dynamic Range

Table 1. Option 230/235/240/245/260/265/280/285/430/435/440/445/460/465/480/485

Description	Specification	SPD	
System dynamic range^{1,2}			
9 kHz to 300 kHz		72 dB	
300 kHz to 10 MHz	IF bandwidth = 3 kHz	82 dB	
10 MHz to 6 GHz		98 dB	
6 GHz to 8.5 GHz		92 dB	
9 kHz to 300 kHz		97 dB	115 dB
300 kHz to 10 MHz	IF bandwidth = 10 Hz	107 dB	115 dB
10 MHz to 6 GHz		123 dB	130 dB
6 GHz to 7 GHz		117 dB	128 dB
7 GHz to 8 GHz		117 dB	126 dB
8 GHz to 8.5 GHz		117 dB	124 dB

Figure 1. System dynamic range (specification and actual measurement data example, IF bandwidth 10 Hz)



1. The test port dynamic range is calculated as the difference between the test port rms noise floor and the source maximum output power. The effective dynamic range must take measurement uncertainty and interfering signals into account.
2. The specification might not be met at 5 MHz or 50 MHz.

System Dynamic Range (continued)

Table 2. Option 2D5/2K5/4D5/4K5

Description	Specification	SPD
System dynamic range^{1,2}		
300 kHz to 1 MHz	70 dB	
1 MHz to 10 MHz	82 dB	
10 MHz to 100 MHz	95 dB	
100 MHz to 6 GHz	IF bandwidth = 3 kHz	98 dB
6 GHz to 8.5 GHz		92 dB
8.5 GHz to 10.5 GHz		80 dB
10.5 GHz to 15 GHz		75 dB
15 GHz to 20 GHz		71 dB
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300 kHz to 1 MHz	95 dB	105 dB
1 MHz to 10 MHz	107 dB	115 dB
10 MHz to 100 MHz	120 dB	129 dB
100 MHz to 6 GHz	IF bandwidth = 10 Hz	123 dB
6 GHz to 8 GHz		117 dB
8 GHz to 8.5 GHz		117 dB
8.5 GHz to 10.5 GHz		105 dB
10.5 GHz to 15 GHz		100 dB
15 GHz to 20 GHz		96 dB

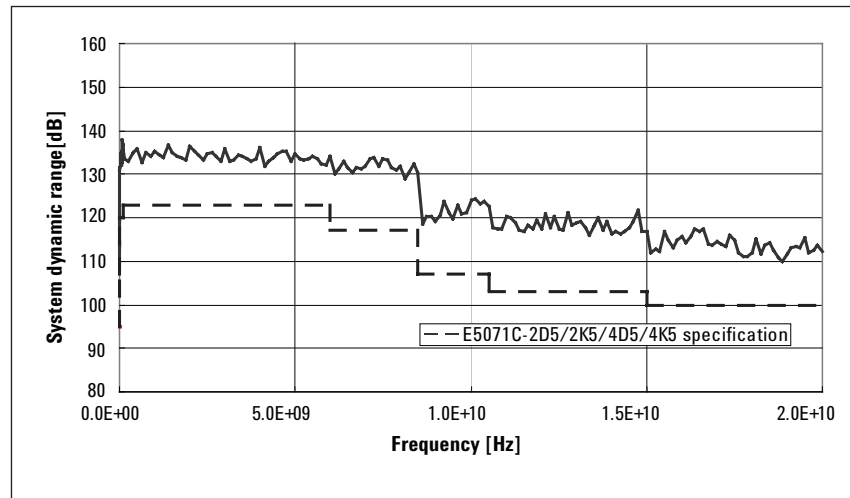


Figure 2. System dynamic range (specification and actual measurement data example, IF bandwidth 10 Hz)

1. The test port dynamic range is calculated as the difference between the test port's rms noise floor and the source's maximum output power. Effective dynamic range must take measurement uncertainty and interfering signals into account.
2. The specification might not be met at 5 MHz or 50 MHz.

Ordering Information

ENA Option TDR software ordering information

Option	Description
E5071C-TDR	Enhanced Time Domain Analysis Option

Option	Description
E5008A-1FP ¹	Add option E5071C-TDR
E5009A-1FP ¹	Upgrade from option E5071C-010 to E5071C-TDR

1. Requires installation and adjustment at local Keysight Service Center.

Typical system configuration

4-port 8.5 GHz system

Qty	Default Options	Available Options	Description
1	E5071C-480		4-port test set, 9 kHz to 8.5 GHz without bias tees
1	E5071C-TDR		Enhanced Time Domain Analysis Software
1		N4431B-010	4-port, 9 kHz to 13.5 GHz 4 x 3.5mm (f) Ecal module
4		1250-1744	3.5mm (f) to Type-N (m) adaptors
4		11500E	Test port cables, APC 3.5mm(m), 24in
1		N1020A	6 GHz Single-ended TDR Probe

4-port 20 GHz system

Qty	Default Options	Available Options	Description
1	E5071C-4K5		4-port test set, 300 kHz to 20 GHz with bias tees
1	E5071C-TDR		Enhanced Time Domain Analysis Software
1		N4433A-010	4-port, 300 kHz to 20 GHz 4 x 3.5mm (f) Ecal module
4		85130-60005	NMD-3.5mm to PSC-3.5mm (f) adaptors
4		11500E	Test port cables, APC 3.5mm(m), 24in
1		N1021B	18 GHz Differential TDR Probe Kit

